AMENDMENTS TO THE CLAIMS

Claims 1-36 are pending in this application. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A memory array with byte-alterable capability comprising:

a select gate metal oxide semiconductor field effect transistor, MOSFET device, and

a split-gate memory cell whose source is connected to the drain of said select gate MOSFET device.

2. (Original) The memory array with byte-alterable capability of claim 1 further comprising:

bit lines which are tied to the drains of said split-gate memory cell.

3. (Original) The memory array with byte-alterable capability of claim 1 further comprising:

source lines which are tied to the sources of said select gate MOSFET devices.

4. (Original) The memory array with byte-alterable capability of claim 1 further comprising:

word lines which are tied to control gates of said split-gate memory cell.

5. (Original) The memory array with byte-alterable capability of claim 1 further comprising:

select lines which are tied to select gates of said select gate MOSFET devices.

6. (Original) The memory array with byte-alterable capability of claim 1 wherein said control gate MOSFET contains a floating gate which is insulated from said control gate by a dielectric insulating material such as silicon dioxide.

7. (Original) The memory array with byte-alterable capability of claim 6 wherein said split-gate memory cell contains a source region which is also the drain for said select gate MOSFET device.

8. (Original) The memory array with byte-alterable capability of claim 6 wherein said control gate MOSFET contains a drain region.

9. (Original) The memory array with byte-alterable capability of claim 6 wherein said control gate MOSFET contains a control gate which is insulated from said floating gate by a dielectric insulating material such as silicon dioxide.

10. (Original) The memory array with byte-alterable capability of claim 6 wherein said control gate contained in the control gate MOSFET device is insulated from said drain of said control gate MOSFET device by a dielectric insulating material.

11. (Original) The memory array with byte-alterable capability of claim 1 wherein said select gate MOSFET contains a select gate which is insulated from said select gate drain region and said selected gate source region by a dielectric insulating material.

12. (Original) The memory array with byte-alterable capability of claim 1 wherein said bits of said bytes have a common source line.

13. (Original) The memory array with byte-alterable capability of claim 1 wherein said source lines common to said bytes have a high voltage applied to inhibit erase of said cells of said unselected bytes.

14. (Original) The memory array with byte-alterable capability of claim 1 wherein said source lines common to said bytes have a low voltage applied to enable an erase of said cells of said unselected bytes.

15. (Original) The memory array with byte-alterable capability of claim 1 wherein the erasure of selected bytes requires a high voltage on said selected gates.

16. (Original) The memory array with byte-alterable capability of claim 1 wherein the erasure of selected bytes requires a high voltage on said control gates.

17. (Original) The memory array with byte-alterable capability of claim 1 wherein the programming of selected cells of said selected bytes require high voltage on said select gate, a lower voltage on said control gate and a high voltage on said source line.

18. (Original) The memory array with byte-alterable capability of claim 1 wherein said word lines common to said bytes have a zero voltage applied to inhibit programming of unselected cells.

19. (Original) A method of producing a memory array with byte-alterable capability comprising the steps of:

including a select gate metal oxide semiconductor field effect transistor, MOSFET device, and

including a split-gate memory cell whose source is connected to the drain of said select gate MOSFET device.

20. (Original) The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

including bit lines which are tied to the drains of said control gate MOSFET devices.

21. (Original) The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

including source lines which are tied to the sources of said select gate MOSFET devices.

22. (Original) The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

including word lines which are tied to control gates of said control gate MOSFET devices.

23. (Original) The method of producing a memory array with byte-alterable capability of claim 19 further comprising the step of:

select lines which are tied to select gates of said select gate MOSFET devices.

24. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein said control gate MOSFET contains a floating gate which is insulated from said control gate by a dielectric insulating material such as silicon dioxide.

25. (Original) The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate MOSFET contains a source region which is also the drain for said select gate MOSFET device.

26. (Original) The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate MOSFET contains a drain region.

27. (Original) The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate MOSFET contains a control gate which is insulated from said floating gate by a dielectric insulating material such as silicon dioxide.

28. (Original) The method of producing a memory array with byte-alterable capability of claim 24 wherein said control gate contained in the control gate MOSFET device is insulated from said drain of said control gate MOSFET device by a dielectric insulating material.

29. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein said select gate MOSFET contains a select gate which is

insulated from said select gate drain region and said select gate source region by a dielectric insulating material.

30. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein said bits of said bytes have a common source line.

31. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein said source lines common to said bytes have a high voltage applied to inhibit erase of said cells of said unselected bytes.

32. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein said source lines common to said bytes have a low voltage applied to enable an erase of said cells of said unselected bytes.

33. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein the erasure of selected bytes requires a high voltage on said select gates.

34. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein the erasure of selected bytes requires a high voltage on said control gates.

35. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein the programming of selected cells of said selected bytes

require high voltage on said select gate, a lower voltage on said control gate and a high voltage on said source line.

36. (Original) The method of producing a memory array with byte-alterable capability of claim 19 wherein said word lines common to said bytes have a zero voltage applied to inhibit programming of unselected cells.

37. (New) A method for inhibiting at least one target memory cell among a group of selected memory cells, wherein each of said memory cell has a select gate transistor whose drain is connected to a source of a split-gate memory cell, said method comprising:

turning on select gate transistors for both said target memory cell and said selected memory cells; and

applying an inhibiting voltage to a target source of a target select gate transistor of said target memory cell to couple said inhibiting voltage to a target drain of a target split-gate memory cell, the coupled inhibiting voltage neutralizing a target floating gate from a electric field created by a target control gate of said target split-gate memory cell.

38. (New) The method of claim 37 further comprising applying an erasing voltage to all control gates of said split-gate memory cells for both said selected memory cell and said target memory cell.

39. (New) The method of 38 wherein said erasing voltage is higher than said inhibiting voltage.

40. (New) The method of claim 39 further comprising applying a low voltage

to all selected sources of said select gate transistors for said selected memory cells, wherein said inhibiting voltage is higher than said low voltage.

41. (New) The method of claim 37 further comprising applying a programming voltage to all control gates of said split-gate memory cells for both said selected memory cell and said target memory cell.

42. (New) The method of 41 wherein said programming voltage is lower than said inhibiting voltage.

43. (New) The method of claim 42 further comprising applying a high voltage to all selected sources of said select gate transistors for said selected memory cells, wherein said inhibiting voltage is lower than said high voltage.